GR 400 D 64 L3 2GDC

- GR — GOODRAM
- 400 — SPEED / DATA TRANSFER 400MHz / PC-3200
- D — MODULE TYPE DDR SDRAM DIMM
- 64 — MODULE DATA WIDTH 64
- L3 — CAS LATENCY 3
- 2GDC — MODULE DENSITY 2GB DUAL CHANNEL

DDR MODULE PART NUMBERING SYSTEM

GOOD RAM professional memory for everyone

FEATURES

PART NUMBER	GR400D64L3/2GDC
MODULE TYPE	DDR SDRAM DIMM
MODULE DENSITY	2x1GB
MODULE DATA WIDTH	64
DRAM CHIP ORAGNIZATION	64Mx8
NUMBER OF DRAM CHIPS	16
NUMBER OF MODULE RANKS	2
NUMBER OF MODULE SIDES	2
REGISTERED	NO
ECC SUPPORT	NO
PIN COUNT	184 PIN
SUPPLY VOLTAGE	2,6V
SSTL_2 COMPATIBLE	YES
PROGRAMMED SPD MEMORY	128 BYTES
MAX AVG PERIODIC REFRESH INTERVAL	7,8 s

OPERATING FREQUENCY — CAS Latency

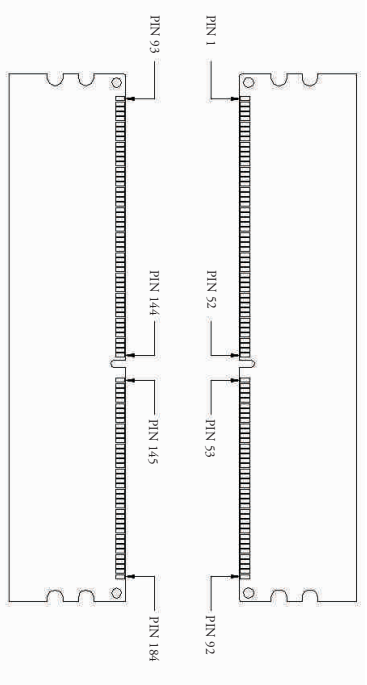
400MHz (2x200MHz) | PC-3200	3
333MHz (2x166MHz) | PC-2700	2,5
266MHz (2x133MHz) | PC-2100	2

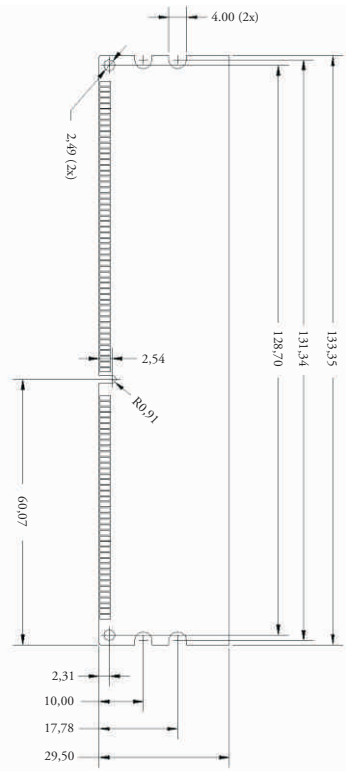
DYNAMIC PARAMETERS FOR 400MHz

RAS# TO CAS# DELAY, tRCD	15 ns
ROW PRECHARGE TIME, tRP	15 ns
ROW ACTIVE TO ROW ACTIVE DELAY, tRRD	10 ns
ACTIVE TO PRECHARGE TIME, tRAS	40 ns
ACTIVE TO ACTIVE / AUTO REFRESH TIME, tRC	55 ns
AUTO REFRESH TO ACTIVE / AUTO REFRESH, tRFC	65 ns
DEVICE CYCLE TIME, tCK MAX	10

PCB DETAILS

PCB TYPE	DDR SDRAM DIMM
BOARD DIMENSIONS	133,35 x 29,5mm ± 0,1mm
BOARD THICKNESS	1,27mm ± 0,13mm
DRAM PACKAGE INFORMATION	TSOP, x8bit
CONTACT PADS (PIN)	GOLD PLATED





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SPD CONFIGURATION

BYTE	DESCRIPTION	HEX	DEC
0	Number of Serial PD Bytes written during module production	0x80	128
1	Total number of Bytes in Serial PD device	0x08	8
2	Fundamental Memory Type (FPM, EDO, SDRAM …)	0x07	7
3	Number of Row Addresses on this assembly	0x0D	13
4	Number of Column Addresses on this assembly	0x0B	11
5	Number of DIMM Banks	0x02	2
6	Data Width of this assembly	0x40	64
7	Data Width of this assembly	0x00	0
8	Voltage Interface Level of this assembly	0x04	4
9	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X	0x50	80
10	SDRAM Access from Clock	0x70	112
11	DIMM configuration type (Non-parity, Parity or ECC)	0x00	0
12	Refresh Rate/Type	0x82	130
13	Primary SDRAM Width	0x08	8
14	Error Checking SDRAM Width	0x00	0
15	SDRAM Device Attributes: Minimum Clock Delay, Back-to-Back RCA	0x01	1
16	SDRAM Device Attributes: Burst Lengths Supported	0x0E	14
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	0x04	4
18	SDRAM Device Attributes: CAS Latency	0x1C	28
19	SDRAM Device Attributes: CS Latency	0x01	1
20	SDRAM Device Attributes: Write Latency/DIMM Type Information	0x02	2
21	SDRAM Module Attributes	0x20	32
22	SDRAM Device Attributes: General	0x01	1
23	Minimum Clock Cycle at CL = X - 0.5	0x60	96
24	Maximum Data Access Time (tAC) from Clock at CL = X - 0.5	0x70	112
25	Minimum Clock Cycle at CL = X - 1	0x75	117
26	Maximum Data Access Time (tAC) from Clock at CL = X - 1	0x75	117
27	Minimum Row Precharge Time (tRP)	0x3C	60
28	Minimum Row Active to Row Active delay (tRRD)	0x28	40
29	Minimum RAS to CAS delay (tRCD)	0x3C	60
30	Minimum Active to Precharge Time (tRAS)	0x28	40
31	Module Bank Density	0x80	128
32	Address and Command Input Setup Time Before Clock	0x60	96
33	Address and Command Input Hold Time After Clock	0x60	96
34	Data Input Setup Time Before Clock	0x40	64
35	Data Input Hold Time After Clock	0x40	64
36	Write recovery time (tWR)	0x00	0
37	Internal write to read command delay (tWTR)	0x00	0
38	Internal read to precharge command delay (tRTP)	0x00	0
39	Memory Analysis Probe Characteristics	0x00	0
40	Extension of Byte 41 tRC and Byte 42 tRFC	0x00	0
41	SDRAM Device Minimum Active to Active/Auto Refresh Time (tRC)	0x37	55
42	SDRAM Device Minimum Auto Refresh to Active/Auto Refresh (tRFC)	0x41	65
43	SDRAM Device Maximum device cycle time (tCKmax)	0x28	40
44	SDRAM Device Maximum skew between DQS and DQ signals (tDQSQ)	0x28	40
45	DDR SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0x50	80
46	Reserved for future use	0x00	0
47	SDRAM Device Attributes - DDR SDRAM DIMM Height	0x00	0
48	Reserved for future use	0x00	0
49	Reserved for future use	0x00	0
50	Reserved for future use	0x00	0
51	Reserved for future use	0x00	0
52	Reserved for future use	0x00	0
53	Reserved for future use	0x00	0
54	Reserved for future use	0x00	0
55	Reserved for future use	0x00	0
56	Reserved for future use	0x00	0
57	Reserved for future use	0x00	0
58	Reserved for future use	0x00	0
59	Reserved for future use	0x00	0
60	Reserved for future use	0x00	0
61	Reserved for future use	0x00	0
62	SPD Revision	0x11	17
63	Checksum for Bytes 0-62	0xF5	245
64-255	Manufacturer's specific data		

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